REMARKS

Claims 7 and 8 have been rewritten in independent form, and are now believed to be allowable, as indicated by the Examiner.

Claims 5 and 6 stand rejected under 35 U.S.C. ə 103(a) as being unpatentable over Yamazaki et al. (U.S. 6,603,453) in view of Yamazaki et al. (US 2001/0052950 A1)

Applicants respectfully traverse this rejection because the cited references, even if combined, still would not disclose or suggest at least the second gate insulation film being formed on the first gate insulation film. The combination also would not disclose or suggest the second gate electrode being formed between the first gate insulation film and the second gate insulation film. Moreover, it would not have been obvious to combine the cited references to derive the claimed semiconductor layer being formed on a substrate.

As shown below in the annotated Fig. 5c, the first thin film transistor (TFT) includes a first gate insulation film which is formed on a semiconductor layer (236,237), a second gate insulation film formed on the first gate insulation film, and the first gate electrode is formed on the second gate insulation film. In contrast, Fig. 16 of Yamazaki '453 (reproduced below) shows that an active layer 806 or 807 is formed between the first gate insulation and a second gate insulation film. Accordingly, the second gate insulation film cannot be formed on the first gate insulation film as in the present invention.

Referring again to Fig. 5c reproduced below, the second thin film transistor of the present invention includes a second gate electrode which is formed between the first gate insulation film and the second gate insulation film. In contrast, Fig. 16 of Yamazaki '453 shows that the active layer is formed between the first gate insulation film and the second gate insulation film. Therefore, a second gate electrode cannot be formed between the first and second insulation film in Yamazaki '453, as is in the present invention. Since the Yamazaki et al. ('950) also does not disclose these features of the present invention, even if it is combined with the Yamazaki et al. '453 reference, they still would not disclose or suggest these features. The present invention is believed allowable for these reasons alone.

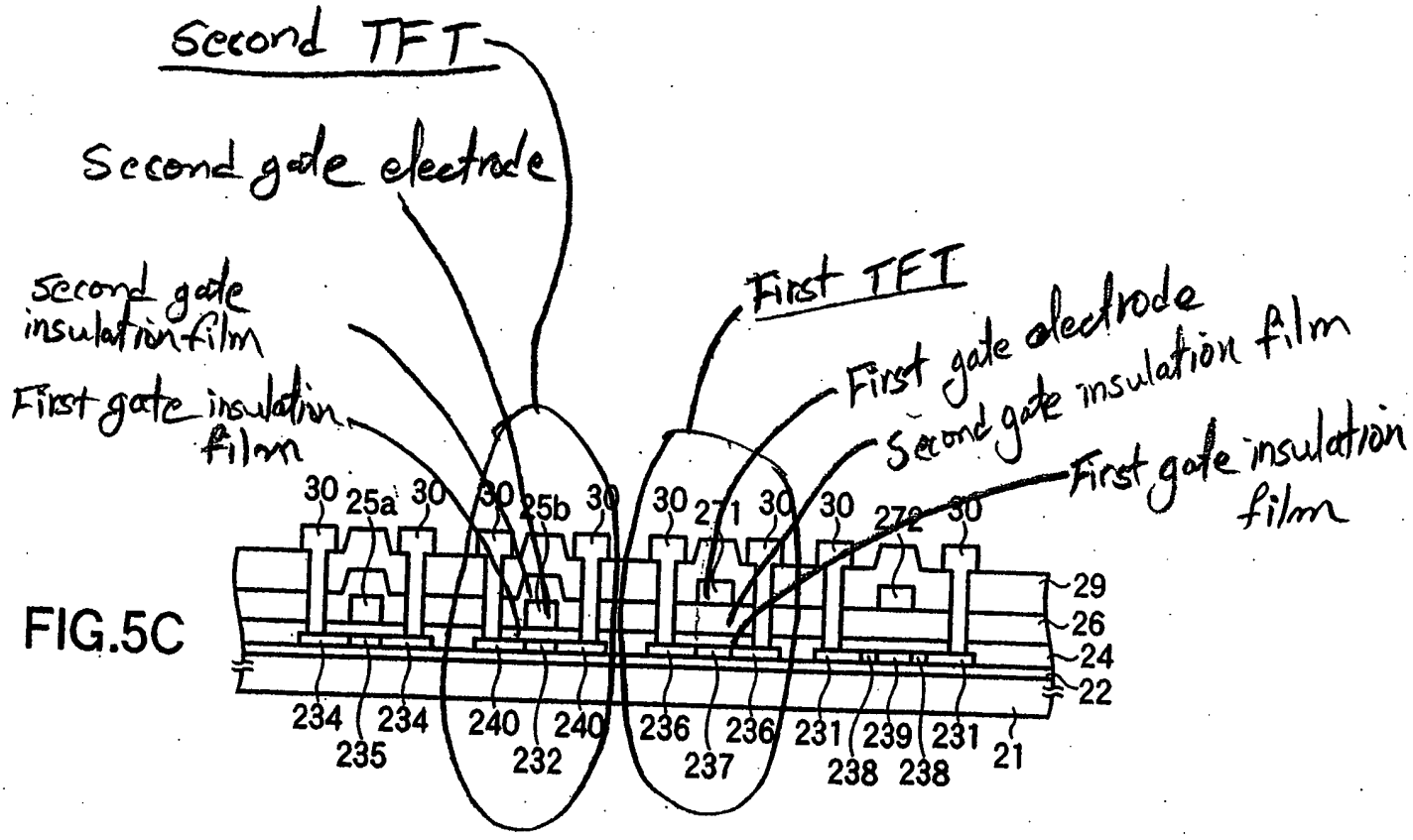
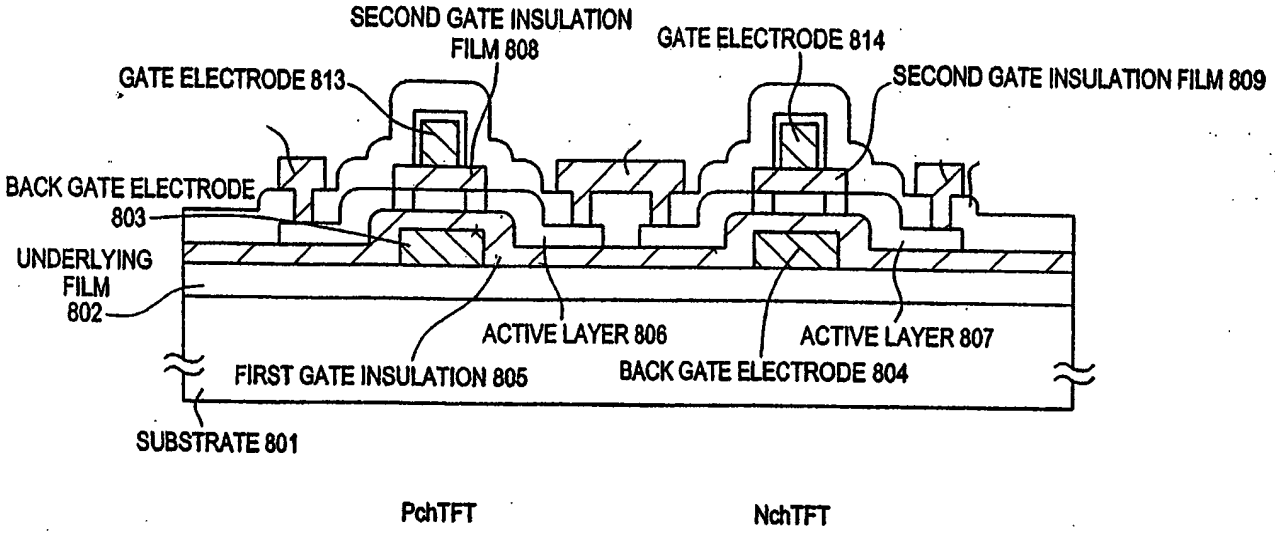


FIG.5C

PRESENT INVENTION

FIG. 16



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Moreover, it would not have been obvious to one of ordinary skill in the art to combine Yamazaki et al. '950 with Yamazaki et al. '453 to derive the feature in which the semiconductor layer is formed on the substrate. Yamazaki '453 relates to a TFT which includes a gate electrode and also a back gate electrode, which is formed directly on the substrate of the TFT. The back gate electrode requires that it be insulated from the active or semiconductor layer. Therefore, it would not be workable to provide a semiconductor layer on the substrate of Yamazaki '453 because of the back gate electrode. The present invention is allowable for this reason also.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

B. Joe Kim
Registration No. 41,895

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Suite 2500
300 South Wacker Drive
Chicago, Illinois 60606
(312) 360-0080
Customer No. 24978
P:\DOCS\1324\68134\S44939.DOC